Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.009 x .009”**

**.026”**

**.026”**

**Top Material: Cr AgAu**

**Backside Material: Cr AgAu**

**Bond Pad Size: .009” X .009”**

**Backside Potential: Cathode**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .026” X .026” DATE: 11/3/21**

**MFG: MOTOROLA THICKNESS .010” P/N: 1N4627**

**DG 10.1.2**

#### Rev B, 7/19/02